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Docket No.
14872

Application Of: **Toshimichi Kurihara et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/942,445	August 30, 2001	Nema O. Berezny	23389	2813	7920

Title: **SEMICONDUCTOR DEVICE IN A RESIN SEALED PACKAGE WITH A RADIATING PLATE AND MANUFACTURING METHOD THEREOF**

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APPEAL BRIEF



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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Applicant: Toshimichi Kurihara, et al.

Examiner: Laura M. Schillinger

Serial No.: 09/942,445

Art Unit: 2813

Filed: August 30, 2001

Docket: 14872

For: SEMICONDUCTOR DEVICE IN A
RESIN SEALED PACKAGE WITH A
RADIATING PLATE AND
MANUFACTURING METHOD THEREOF

Dated: December 6, 2006

Conf. No.: 7920

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APPEAL BRIEF

I. Statement of Real Party in Interest

The real party in interest of the present application is NEC Compound Semiconductor Devices, Ltd., the assignee of the entire right, title and interest in the above-identified patent application.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

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Dated: December 6, 2006



Paul J. Esatto, Jr.

II. Statement of Related Appeals and Interferences

No other appeals and interferences are known which directly affect, or will be directly affected by, or have a bearing on, the disposition of the pending appeal.

III. Statement of Status of Claims

Claim 1 stands rejected based on 35 U.S.C. §103(a) under U.S. Patent No. 5,270,262 to Switky et al. and U.S. Patent No. 5,266,739 to Yamauchi.

Claim 2 is cancelled.

Claim 3 stands rejected based on 35 U.S.C. §103(a) under U.S. Patent No. 5,270,262 to Switky et al. and U.S. Patent No. 5,266,739 to Yamauchi.

Claim 4 is cancelled.

Claim 5 stands rejected based on 35 U.S.C. §103(a) under U.S. Patent No. 5,270,262 to Switky et al. and U.S. Patent No. 5,266,739 to Yamauchi.

Claim 6 is cancelled.

Claim 7 stands rejected based on 35 U.S.C. §103(a) under U.S. Patent No. 5,270,262 to Switky et al. and U.S. Patent No. 5,266,739 to Yamauchi.

Claim 8 is cancelled.

Claim 9 stands rejected based on 35 U.S.C. §103(a) under U.S. Patent No. 5,270,262 to Switky et al. and U.S. Patent No. 5,266,739 to Yamauchi.

Claim 10 is cancelled.

Claim 11 stands rejected based on 35 U.S.C. §103(a) under U.S. Patent No. 5,270,262 to Switky et al. and U.S. Patent No. 5,266,739 to Yamauchi.

Claim 12 is cancelled.

Claim 13 stands rejected based on 35 U.S.C. §103(a) under U.S. Patent No. 5,270,262 to Switky et al. and U.S. Patent No. 5,266,739 to Yamauchi.

Claim 14 is cancelled.

Claim 15 stands rejected based on 35 U.S.C. §103(a) under U.S. Patent No. 5,270,262 to Switky et al. and U.S. Patent No. 5,266,739 to Yamauchi.

Claim 16 is cancelled.

Claim 17 is allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

Claim 18 is cancelled.

Claim 19 is withdrawn pursuant to a Restriction Requirement mailed on September 11, 2002.

Claim 20 is withdrawn pursuant to a Restriction Requirement mailed on September 11, 2002.

Claim 21 is withdrawn pursuant to a Restriction Requirement mailed on September 11, 2002.

Claim 22 stands rejected based on 35 U.S.C. §103(a) under U.S. Patent No. 5,270,262 to Switky et al. and U.S. Patent No. 5,266,739 to Yamauchi.

Claim 23 is cancelled.

Claim 24 stands rejected based on 35 U.S.C. §103(a) under U.S. Patent No. 5,270,262 to Switky et al. and U.S. Patent No. 5,266,739 to Yamauchi.

Claim 25 is cancelled

IV. Statement of Status of Amendments

No amendments were made subsequent to the final rejection.

V. Summary of Claimed Subject Matter

The invention with respect to claim 1 comprises a radiating plate (e.g., See: FIG. 3, ref. 20; page 7, line 13; page 18, line 22), a semiconductor chip bonded onto the radiating plate (e.g., See: FIG. 3, ref. 1; FIG. 8A-8C, ref. 1; page 7, line 14; page 21, lines 26-27), a rectangular-shaped resin wall that surrounds the semiconductor chip (e.g., See: FIG. 3, ref. 40; FIG. 8A-8C, ref. 40; page 7, lines 14-16; page 21, line 27 – page 22, line 1) and has a first and second pair of opposing sides (e.g., See: FIG. 3, ref. 40), a conductive member (e.g., See: FIG. 3, ref. 30; FIG. 8A-8C, ref. 30) extending through one of the first pair of opposing sides of the resin wall and retained by the resin wall (e.g., See: FIG. 3; FIG. 8A-8C; page 7, lines 17-19; page 22, lines 2-20), where the conductive member is electrically connected to the semiconductor chip (e.g., See: FIG. 3, FIG. 8A; page 7, lines 17-19; page 22, lines 21-23), and a resin lid (e.g., See: FIG. 3, ref. 50; FIGS. 8B-8C, ref. 50) bonded to an upper end of the resin wall (e.g., See: FIG. 3; FIG. 8B-8C; page 7, lines 19-22; page 18, lines 22-23; page 22, lines 24-28), where the semiconductor chip is sealed in a space enclosed by the radiating plate, resin wall and resin lid (e.g., See: FIG. 3; FIG. 8B-8C; page 7, lines 19-22; page 18, lines 22-23; page 23, lines 1-8), and the radiating plate extends outward of the second pair of opposing sides of the resin wall (e.g., See: FIG. 3; FIG. 8A).

The invention with respect to claim 3 comprises the elements identified with respect to claim 1 above, and further, wherein the resin wall is fitted to protruding parts (e.g., See: FIG. 4, ref. 24; FIG. 5, ref. 24; page 19, line 16-23) or recessed parts provided on the radiating plate (e.g., See: FIGS. 4-5; page 19, line 28 – page 20, line 15).

The invention with respect to claim 5 comprises the elements identified with respect to claim 3 above, and further, wherein the recessed parts are provided on the opposed side parts of

the radiating plate, the protruding parts are protruded and provided on the inner surfaces of the recessed parts, and the lower end part of the resin wall is buried in the recessed parts (e.g., See: FIGS. 4-5; page 20, lines 10-15).

The invention with respect to claim 7 comprises the elements identified with respect to claim 1 above, and further, wherein holes (e.g., See: FIGS. 3, 5, 6, 8A, 8C, ref. 31) are provided in the conductive member and the holes are located in the outside positions of the resin wall on the conductive member (e.g., See: FIGS. 3, 5, 6, 8A, 8C, ref. 31; page 20, lines 24-25).

The invention with respect to claim 9 comprises the elements identified with respect to claim 1 above, and further, wherein first holes (e.g., See: FIGS. 3, 6, 8A, 8C, ref. 31) are provided in the conductive member and the first holes are located in the outside positions of the resin wall on the conductive member (e.g., See: FIGS. 3, 8A, 8C, ref. 31; page 20, lines 24-25), and second holes (e.g., See: FIGS. 3, 6, 8A, 8C, ref. 32) or cutouts (e.g., See: FIGS. 6 and 8A, ref. 33) are provided in the region extending through the resin wall of the conductive member (e.g., See: FIGS. 3, 8A, 8C; page 21, lines 1-3; page 22, lines 4-9).

The invention with respect to claim 11 comprises the elements identified with respect to claim 9 above, and further, wherein the first holes (e.g., See: FIG. 12, ref. 71) are arranged so as to overlap the space area between the second holes (e.g., See: FIG. 12, ref. 72) or cutouts (e.g., See: FIG. 12, ref. 73; page 26, lines 15 – 22) when the conductive member is seen in the resin wall direction from the outside of the resin wall.

The invention with respect to claim 13 comprises the elements identified with respect to claim 1 above, and further, wherein a stepped part (e.g., See: FIGS. 7A-7C, ref. 53) to be fitted to the inner periphery of the resin wall is provided on the resin lid (e.g., See: FIGS. 7A-7C and 8C; page 21, lines 10-18).

The invention with respect to claim 15 comprises the elements identified with respect to claim 13 above, and further, wherein the resin lid has a vertically plane symmetric shape (e.g., See: FIGS. 7A-7C and 8C; page 21, lines 7-9).

The invention with respect to claim 17 comprises the elements identified with respect to claim 1 above, and further, wherein the surface of the radiating plate surrounded by the resin wall is surface-finished by silver plating, and the other surface of the radiating plate except the part for bonding the resin wall and the inner lead part and outer lead part of the conductive member are surface finished by gold plating (e.g., See: FIGS. 11A-11D; page 20, lines 19-24; page 24, line 9 – page 25, line 9).

The invention with respect to claim 22 comprises the elements identified with respect to claim 1 above, and further, wherein the radiating plate has end portions (e.g., See: FIG. 4, ref. 21 and 23; page 19, lines 16-18) formed integrally at both ends of a center portion (e.g., See: FIG. 4, ref. 22; page 19, lines 16-18) of the radiating plate, the lower end of the resin wall is bonded to the center portion, and the end portions are exposed through the resin wall (e.g., See: FIG. 5; page 19, line 16 – page 20, line 15).

The invention with respect to claim 24 comprises the elements identified with respect to claim 1 above, and further, wherein the conductive member is broader on the inside of the resin wall (e.g., See: FIGS. 6 and 8A, ref. 30a; page 22, lines 10-20).

VI. Statement of Grounds of Rejection to be Reviewed on Appeal

1. Rejection under 35 U.S.C. §103(a) based on U.S. Patent No. 5,270,262 to Switky et al. (hereinafter “Switky”) and U.S. Patent No. 5,266,739 to Yamauchi (hereinafter “Yamauchi”).

VII. Statement of Argument

A. Claim 1

This obviousness rejection relies on the combined disclosures of Switky and Yamauchi, in combination, for allegedly disclosing the semiconductor device recited in claim 1 on appeal.

Appellant respectfully submits that claim 1 on appeal is not obvious from the above combination of references since neither of the references, individually or in combination, teaches or suggests applicants' claimed semiconductor device as recited in claim 1.

The present invention, as recited in independent claim 1, and as shown in Fig. 3, teaches a semiconductor device 12 comprising a radiating plate 20, a semiconductor chip 1 bonded onto the radiating plate 20, and a rectangular-shaped resin wall 40 which surrounds the semiconductor chip 1 bonded to the radiating plate 20. The rectangular-shaped resin wall 40 has a first pair of opposing sides and a second pair of opposing sides. The semiconductor device 12 further comprises a conductive member 30 extending through one of the first pair of opposing sides of the resin wall 40 and retained by the resin wall 40, where the conductive member 30 is electrically connected to the semiconductor chip 1, and a resin lid 50 bonded to an upper end of the resin wall 40, where the semiconductor chip 1 is sealed in a space enclosed by the radiating plate 20, resin wall 40 and resin lid 50. The radiating plate 20 extends outward of the second pair of opposing sides of the resin wall 40.

Switky, in Figs. 1-3, 5 and 7, discloses a semiconductor chip 16 placed on a bonding pad 17, which is attached to bottom plate 14. Plastic beads 15 are provided on the outer portions of the bottom plate 14 and of top plate 11. However, it is clear that the plastic beads 15 (alleged by the Examiner to be the rectangular-shaped resin wall of the present invention) are oval-shaped beads, not a "rectangular-shaped resin wall" as alleged by the Examiner.

As shown in Figs. 8A to 8C of the present invention, the semiconductor chip 1 is bonded to the center of the radiating plate 20. The rectangular-shaped resin wall 40 surrounds the circumference of the semiconductor chip 1 and is bonded at the lower end to the radiating plate 20. The lead 30 is extended through the rectangular-shaped resin wall 40 and retained by the rectangular-shaped resin wall 40.

Furthermore, the present invention recites a rectangular-shaped resin wall 40, having a first pair of opposing sides and a second pair of opposing sides, similar to any rectangle. A conductive member 30 extends outward of the first pair of opposing sides of the rectangular-shaped resin wall 40, and the conductive member 30 is retained by the rectangular-shaped resin wall 40. The radiating plate 20 extends outward of the second pair of opposing sides of the rectangular-shaped resin wall 40. As Switky fails to even teach a rectangular-shaped resin wall, and only teaches oval plastic beads 15, Switky further fails to teach a conductive member extending outward of a first pair of opposing sides and a radiating plate extending outward of the second pair of opposing sides.

The additional cited reference of Yamauchi is only cited by the Examiner to teach that the lid of the present invention is a “resin” lid. Yamauchi teaches just this feature, if that, and completely fails to teach any other element of the claims as recited above. The remaining teachings of the Yamauchi reference is completely irrelevant to the present invention, and it is unlikely that one of ordinary skill in the art would even look to the Yamauchi reference to solve the shortcomings of the prior art as solved by the present invention. Even if one were to take the teachings of Yamauchi and combine it with Switky, the combination would fail to render the claim limitations obvious.

It has been held by the Courts that to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). The combination of Switky and Yamauchi made by the Examiner completely fails to teach a semiconductor device having a rectangular-shaped resin wall that surrounds a semiconductor chip bonded to a radiating plate, and has a first and second pair of opposing sides, where a conductive member extends through the first pair of opposing sides and the radiating plate extends outward of the second pair of opposing sides of the resin wall, and where the semiconductor chip is sealed in a space enclosed by the radiating plate, resin wall and resin lid.

B. Claims 7, 9 and 11

Regarding claims 7, 9 and 11, the Examiner alleges that Switky discloses first holes in the outside positions of the resin wall on the conductive member, and second holes in the region extending through the resin wall of the conductive member, wherein the first holes overlap the space area between the second holes. As shown in Fig. 3 of the present invention, the semiconductor device 12 is a resin-sealed package equipped with a radiating plate, which comprises a semiconductor chip 1, a radiating plate 20, a lead 30, a resin wall 40 and a resin lid 50. The lead 30 has first holes 31 in the outside positions of the resin wall 40. The second holes 32 and cutouts 33 of the lead 30 are provided within the region extending through the resin wall 40 of the lead 30. Namely, the second holes 32 and cutouts 33 are buried in the resin wall 40.

Switky discloses holes (element 23) on the lead 13 in Fig. 5 outside of the plastic beads 15. However, Switky completely fails to disclose second holes provided in the region extending through the resin wall of the conductive member, as recited in claims 9 and 11.

C. Claim 22

Regarding claim 22, the Examiner alleges that Switky discloses a radiating plate that has end portions formed integrally at both ends of a center portion of a radiating plate, where the lower end of the resin wall is bonded to the center portion of the radiating plate, and the end portions are exposed through the resin wall. The present invention clearly shows, in Fig. 3, that the resin wall 40 is bonded to a center portion of the radiating plate 20, and that end portions of the radiating plate 20 are exposed through the resin wall 40.

Switky, however, shows a radiating plate 14 that has plastic beads 15 at the outer ends of the radiating plate 14. Switky fails to teach that the plastic beads 15 are bonded to a center portion of the radiating plate 14, clearly shown in Fig. 2 of Switky. Further, Switky does not disclose that end portions of the plate 14 are exposed through the plastic beads 15.

D. Claims 3, 5, 13, 15 and 24

Remaining dependent claims 3, 5, 13, 15 and 24 recite additional unique elements and/or limitations, and are allowable for all of the reasons as the claims on which they depend.


VIII. CONCLUSION

It is clear that all of the limitations of claims 1, 3, 5, 7, 9, 11, 13, 15, 22 and 24 are not taught or suggested by the references of Switky and Yamauchi, individually or in combination. Accordingly, Applicant respectfully submits that the Examiner has not met his burden of establishing a prima facie case of obviousness based on the prior art, as required by 35 U.S.C. §103(a)¹; no objective teaching in Switky and Yamauchi, individually or in combination, would lead an individual of ordinary skill in the art to produce the present invention.

The above arguments establish that claims 1, 3, 5, 7, 9, 11, 13, 15, 22 and 24 on appeal are patentable over the combination of Switky and Yamauchi. In view of the remarks set forth in

this Appeal Brief, Appellant respectfully requests that the rejection under 35 U.S.C. §103(a) citing the aforementioned references made in the Final Rejection dated March 31, 2004, and in the Advisory Action of July 21, 2004, be reversed by the Board of Patent Appeals and Interferences.

Respectfully submitted,



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CLAIMS APPENDIX

1. (Previously Presented) A semiconductor device comprising:

a radiating plate;

a semiconductor chip bonded onto the radiating plate;

a rectangular-shaped resin wall which surrounds the semiconductor chip bonded to the radiating plate, said rectangular-shaped resin wall having a first pair of opposing sides and a second pair of opposing sides;

a conductive member extending through one of the first pair of opposing sides of the resin wall and retained by the resin wall, said conductive member is electrically connected to the semiconductor chip; and

a resin lid bonded to an upper end of the resin wall, said semiconductor chip is sealed in a space enclosed by said radiating plate, said resin wall and said resin lid, said radiating plate extends outward of said second pair of opposing sides of said resin wall.

3. (Original) The semiconductor device according to claim 1, wherein the resin wall is fitted to protruding parts or recessed parts provided on the radiating plate.

5. (Previously Presented) The semiconductor device according to claim 3, wherein the recessed parts are provided on the opposed side parts of the radiating plate, the protruding parts are protruded and provided on the inner surfaces of the recessed parts, and the lower end part of the resin wall is buried in the recessed parts.

7. (Previously Presented) The semiconductor device according to claim 1, wherein holes are provided in the conductive member and said holes are located in the outside positions of the resin wall on the conductive member.

9. (Previously Presented) The semiconductor device according to claim 1, wherein first holes are provided in the conductive member and said first holes are located in the outside positions of the resin wall on the conductive member, and second holes or cutouts are provided in the region extending through the resin wall of the conductive member.

11. (Original) The semiconductor device according to claim 9, wherein the first holes are arranged so as to overlap the space area between the second holes or cutouts when the conductive member is seen in the resin wall direction from the outside of the resin wall.

13. (Original) The semiconductor device according to claim 1, wherein a stepped part to be fitted to the inner periphery of the resin wall is provided on the resin lid.

15. (Original) The semiconductor device according to claim 13, wherein the resin lid has a vertically plane symmetric shape.

22. (Previously Presented) The semiconductor device according to claim 1, wherein the radiating plate has end portions formed integrally at both ends of a center portion of the radiating plate, the lower end of the resin wall is bonded to said center portion, and said end portions are exposed through the resin wall.

24. (Previously Presented) The semiconductor device according to claim 1, wherein said conductive member is broader on the inside of said resin wall.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None